Electronic Version
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PHASE FREQUENCY DETECTOR WITH PROGRAMMABLE MINIMUM PULSE WIDTH

Abstract

A structure and associated method for reducing a static phase error in a phase-locked loop circuit. The phase-locked loop circuit comprises a voltage controlled oscillator and a phase frequency detector. The voltage controlled oscillator is adapted to provide a first clock signal comprising a first frequency.The phase frequency detector is adapted to compare the first clock signal comprising the first frequency to a reference clock signal comprising a reference frequency. The phase frequency detector comprises a programmable circuit adapted to vary a minimum pulse width of an increment pulse and a minimum pulse width of a decrement pulse. The programmable circuit is further adapted to reduce a static phase error of the phase locked-loop circuit.